WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed above the semiconductor substrate and having a relative dielectric constant of 3.8 or less;

a conductor which covers a side face of the first insulating film at least near four corners of the semiconductor substrate, and at least an outer side face of which has a conductive barrier layer; and

a second insulating film covering the outer side face of the conductor and having a relative dielectric constant of over 3.8.

2. A semiconductor device as set forth in claim 1, wherein the conductive barrier layer that the conductor has contains one kind selected from a group consisting of titanium (Ti), tantalum (Ta), zirconium (Zr), and tungsten (W), and the conductor contains as a major component one kind selected from a group consisting of copper (Cu), aluminum (Al), and tin (Sn).

3. A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed above the semiconductor substrate and having a relative dielectric constant of 3.8 or less;

a conductor covering a side face of the first insulating film at least near four corners of the semiconductor substrate;

a second insulating film covering an outer side face of the conductor and having a relative dielectric constant of over 3.8; and

a corrosion resistant conductor formed at least near the four

corners of the semiconductor substrate to extend from directly under the second insulating film to directly under the conductor.

4. A semiconductor device as set forth in claim 3, wherein the conductor has one kind selected from a group consisting of copper (Cu), aluminum (Al), and tin (Sn).

5. A semiconductor device as set forth in claim 3, wherein the corrosion resistant conductor is formed along an entire peripheral edge of the semiconductor substrate.

6. A semiconductor device as set forth in claim 3, wherein the corrosion resistant conductor has tungsten (W).

7. A semiconductor device as set forth in claim 1,

wherein the second insulating film also covers an upper side of the first insulating film, the semiconductor device further comprising

a conductor pattern passing through the second insulating film positioned on the upper side of the first insulating film.

8. A semiconductor device as set forth in claim 3,

wherein the second insulating film also covers an upper side of the first insulating film, the semiconductor device further comprising

a conductor pattern passing through the second insulating film positioned on the upper side of the first insulating film.

9. A semiconductor device as set forth in claim 7, further comprising a conductive pattern buried in the first insulating film.

10. A semiconductor device as set forth in claim 8, further comprising a conductive pattern buried in the first insulating film.

11. A semiconductor device as set forth in claim 1, wherein the first insulating film is constituted of a plurality of layers.

12. A semiconductor device as set forth in claim 3, wherein the first insulating film is constituted of a plurality of layers.

13. A semiconductor device as set forth in claim 1, wherein the conductor is formed in a ring shape covering an entire side face of the first insulating film.

14. A semiconductor device as set forth in claim 3, wherein the conductor is formed in a ring shape covering an entire side face of the first insulating film.

15. A semiconductor device as set forth in claim 1, wherein the second insulating film is at least one kind selected from a group consisting of silicon oxide (SiO_2), silicon nitride (SiN), silicon carbide (SiC), and silicon carbonitride (SiCN).

16. A semiconductor device as set forth in claim 3, wherein the second insulating film is at least one kind selected from a group consisting of silicon oxide (SiO_2), silicon nitride (SiN), silicon carbide (SiC), and silicon carbonitride (SiCN).

17. A semiconductor device manufacturing method, comprising:

forming a first insulating film having a relative dielectric constant of 3.8 or less above a semiconductor wafer;

forming trenches at least near an intersecting point of dicing lines on the semiconductor wafer, the trenches facing each other across the dicing line and passing through the first insulating film;

forming a conductor layer in each of the trenches via a conductive barrier layer to fill the trench with the conductor layer;

removing the first insulating film at least near the intersecting point of the dicing lines sandwiched by the trenches

each filled with the conductor layer;

forming a second insulating film having a relative dielectric constant of over 3.8 to cover the conductive barrier layer exposed by the removal of the first insulating film; and

dicing the semiconductor wafer after forming the second insulating film.

18. A semiconductor device manufacturing method as set forth in claim 17, wherein the forming of the first insulating film, the forming of the trenches passing through the first insulating film, and the filling of the trench are repeated a plurality of times.

19. A semiconductor device manufacturing method, comprising:

forming a corrosion resistant conductor layer above a semiconductor wafer at least near an intersecting point of dicing lines on the semiconductor wafer to embrace the dicing lines;

forming a first insulating film having a relative dielectric constant of 3.8 or less above the semiconductor wafer above which the corrosion resistant conductor layer is formed;

forming a trench passing through the first insulating film at least near the intersecting point of the dicing lines on the semiconductor wafer to embrace the dicing lines;

forming a conductor layer in the trench to fill the trench with the conductive layer;

forming a second trench at least near the intersecting point of the dicing lines on the semiconductor wafer to embrace the dicing lines, the second trench passing through the conductor layer to reach the corrosion resistant conductor layer;

forming a second insulating film having a relative dielectric

constant of over 3.8 to cover the conductor layer and the corrosion resistant conductor layer that are exposed in the second trench; and

dicing the semiconductor wafer after forming the second insulating film.

20. A semiconductor device manufacturing method as set forth in claim 19, wherein the forming of the first insulating film, the forming of the trench passing through the first insulating film, and the filling of the trench are repeated a plurality of times.